Exhibit I

5. (Twice Amended) A semiconductor device according to claim [9] 13 wherein said diffusion layer of the first conductivity type is a channel stopper region.

6. (Twice Amended) A semiconductor device according to claim [10] 14 wherein said diffusion layer of the first conductivity type is a channel stopper region.

11. (Amended) A semiconductor device according to claim [9] 13, wherein said transistor is a high voltage transistor, said source diffusion layer and said drain diffusion layer are high impurity concentration, and said source side offset diffusion layer and said drain side offset diffusion layer are lower in impurity concentration than said source diffusion layer and said drain diffusion layer.

12. (Amended) A semiconductor device according to claim [10] 14, wherein said transistor is a high voltage transistor, said source diffusion layer and said drain diffusion layer are high impurity concentration, and said source side offset diffusion layer and said drain side offset diffusion layer are lower in impurity concentration than said source diffusion layer and said drain diffusion layer.